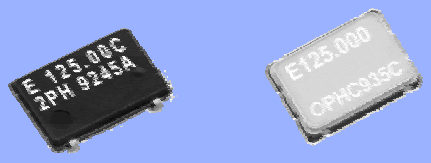
CRYSTAL OSCILLATOR
PROGRAMMABLE

SG-8002JF / CA series

- Frequency range : 1 MHz to 125 MHz
- Supply voltage : 3.3 V or 5.0 V
- Function : Output enable(OE) or Standby($\overline{ST}$)
- Thickness : 1.5 mm Max.
- Pin compatible with ceramic package crystal oscillator (7 × 5) : SG-8002JF
- Short mass production lead time by PLL technology.
- SG-Writer available to purchase. Please contact Epson Toyocom or local sales representative.

Pb Free RoHS Compliant

CA Type Only



Actual size

SG-8002JF	SG-8002CA
	

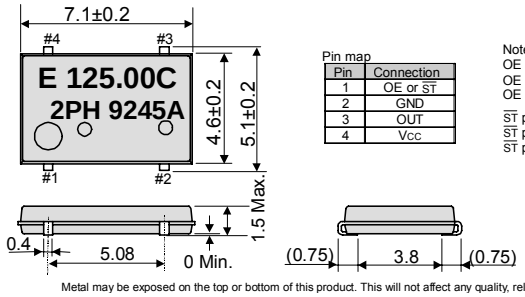
Specifications (characteristics)

Item		Symbol	Specifications *2 PT / ST	PH / SH	PC / SC	Remarks
Output frequency range		f_0	1 MHz to 125 MHz		—	Vcc=4.5 V to 5.5 V
			—		1 MHz to 125 MHz	Vcc=3.0 V to 3.6 V
			—		1 MHz to 66.7 MHz	Vcc=2.7 V to 3.6 V
Supply voltage		Vcc	4.5 V to 5.5 V		2.7 V to 3.6 V	
Temperature range	Storage temperature	T_stg	-55 °C to +125 °C			Store as bare product after unpacking
	Operating temperature	T_use	-20 °C to +70 °C (-40 °C to +85 °C)		-40 °C to +85 °C	Refer to "Outline specifications" (Frequency range)
Frequency tolerance		f_tol(osc)	B: ±50 × 10^{-6} ,C: ±100 × 10^{-6}			-20 °C to +70 °C
			M: ±100 × 10^{-6}			-40 °C to +85 °C *3
Current consumption		Icc	45 mA Max.		28 mA Max.	No load condition, Max. frequency range
Output disable current		I_dis	30 mA Max.		16 mA Max.	OE=GND(PT,PH,PC)
Stand-by current		I_std	50 µA Max.			$\overline{ST}$ =GND(ST,SH,SC)
Symmetry*1		SYM	—	40 % to 60 %		CMOS load:50 % Vcc level, Max. load condition
			40 % to 60 %	—		TTL load: 1.4V level, Max. load condition
High output voltage		VOH	Vcc-0.4 V Min.			IOH=-16 mA(PT / ST,PH / SH),-8 mA(PC / SC)
Low output voltage		VOL	0.4 V Max.			IOL=16 mA(PT / ST,PH / SH), 8 mA(PC / SC)
Output load condition (TTL) *1		L_TTL	5TTL Max.	—		f0≤90 MHz,Max. supply voltage
Output load condition (CMOS) *1		L_CMOS	15 pF Max.	15 pF Max. (CA:25 pF Max.)	15 pF Max.	Max. frequency and Max. supply voltage
Output enable / disable input voltage		VIH	2.0 V Min.		70 % Vcc Min.	$\overline{ST}$, OE terminal
		VIL	0.8 V Max.		20 % Vcc Max.	$\overline{ST}$, OE terminal
Output rise and fall time *1		t_r / t_f	—	3 ns Max.		CMOS load: 20 % Vcc to 80 % Vcc level
			4 ns Max.	—		TTL load: 0.4 V to 2.4 V level
Oscillation start up time		tosc	10 ms Max.			Time at minimum supply voltage to be 0 s
Frequency aging		f_aging	±5 × 10^{-6} / year Max.			+25 °C, Vcc=5.0 V/ 3.3 V (PC / SC) First year

*1 Operating temperature (-40 °C to +85 °C), the available frequency, symmetry and output load conditions, please refer to "Outline specifications" page.
*2 PLL-PLL connection & Jitter specification, please refer to "Jitter specifications and characteristics chart" page.
*3 PT / ST and PH / SH for "M" tolerance will be available up to 55 MHz. (JF:40 MHz)
Checking possible by the Frequency Checking Program.

External dimensions (Unit:mm)

● **SG-8002JF**



Pin map

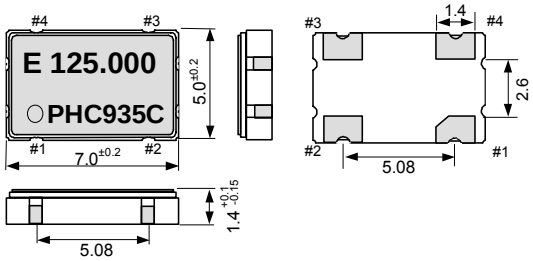
Pin	Connection
1	OE or $\overline{ST}$
2	GND
3	OUT
4	Vcc

Note.
OE Pin (PT, PH, PC)
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.

$\overline{ST}$ pin (ST, SH, SC)
$\overline{ST}$ pin = "H" or "open" : Specified frequency output.
$\overline{ST}$ pin = "L" : Output is low level (weak pull - down), oscillation stops.

Metal may be exposed on the top or bottom of this product. This will not affect any quality, reliability or electrical spec.

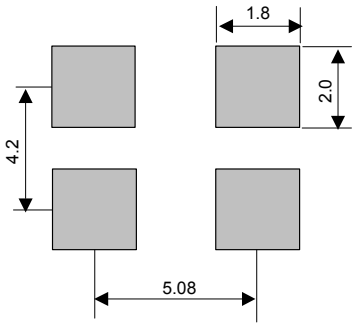
● **SG-8002CA**



Pin map

Pin	Connection
1	OE or ST
2	GND
3	OUT
4	Vcc

Footprint (Recommended) (Unit:mm)



SG / HG-8002 series_ Jitter specifications and characteristics chart

■PLL-PLL connection

Because we use a PLL technology, there are a few cases that the jitter value will increase when SG-8002 is connected to another PLL-oscillator.
In our experience, we are unable to recommend these products for the applications such as telecom carrier use or analog video clock use. Please be careful checking in advance for these application (Jitter specification is Max.250 ps/CL=15 pF)

■Remarks on noise management for power supply line

We do not recommend inserting filters or other devices in the power supply line as the counter measure of EMI noise reduction.
This device insertion might cause high-frequency impedance high in the power supply line and it affects oscillator stable drive.
When this measure is required, please evaluate circuitry and device behavior in the circuit and verify that it will not affect oscillation.
Start up time (0 % Vcc to 90 % Vcc) of power source should be more than 150 µs.

■Jitter Specifications

Model	Supply Voltage	Jitter Item	Specifications	Remarks
PT / PH ST / SH	5.0 V ±0.5 V	Cycle to cycle	150 ps Max.	33 MHz ≤ f0 ≤ 125 MHz, L_CMOS=15 pF
			200 ps Max.	1.0 MHz ≤ f0 < 33 MHz, L_CMOS=15 pF
		Peak to peak	200 ps Max.	33 MHz ≤ f0 ≤ 125 MHz, L_CMOS=15 pF
			250 ps Max.	1.0 MHz ≤ f0 < 33 MHz, L_CMOS=15 pF
SC / PC	3.3 V ±0.3 V	Cycle to cycle	200 ps Max.	1.0 MHz ≤ f0 ≤ 125 MHz, L_CMOS=15 pF
		Peak to peak	250 ps Max.	1.0 MHz ≤ f0 ≤ 125 MHz, L_CMOS=15 pF

■SG-8002 series Characteristics chart